CLAIMS

1. A method of making a charge-coupled device comprising:

forming an electrically conducting charge transfer channel in a semiconductor substrate;

forming an electrically insulating layer on a surface of the substrate;

forming a layer of gate electrode material on the insulating layer;

forming on the gate material layer a first patterned masking layer having apertures that expose regions of the underlying gate material layer that are to form gate electrodes;

electrically doping the first-pattern-exposed regions of the gate material layer;

forming on the gate material layer a second patterned masking layer having apertures that expose regions of the underlying gate material layer that are to form gaps between gate electrodes; and

etching the second-pattern-exposed regions of the gate material layer.

2. The method of claim 1 further comprising removal of the first patterned masking layer after electrically doping first-pattern-exposed regions of the gate material layer.

3. The method of claim 1 further comprising removal of the second patterned masking layer after etching second-pattern-exposed regions of the gate material layer.

4. The method of claim 1 wherein the first-pattern-exposed regions of the gate material layer are electrically doped before the second-pattern-exposed regions of the gate material layer are etched.

5. The method of claim 1 wherein electrically doping first-pattern-exposed regions of the gate material layer comprises ion implantation of a selected electrical dopant into the first-pattern-exposed regions of the gate material layer.

6. The method of claim 1 wherein etching the second-pattern-exposed regions of the gate material layer comprises plasma etching the second-pattern-exposed regions of the gate material layer.

7. The method of claim 1 further comprising heat treating the electrically-doped and etched gate electrode material layer to diffuse the electrical dopant through the gate material layer thickness.

8. The method of claim 7 wherein heat treating the electrically-doped and etched gate electrode material layer comprises annealing the gate material layer.

9. The method of claim 7 wherein heat treating the electrically-doped and etched gate electrode material layer comprises oxidation of the gate material layer.

10. The method of claim 7 wherein forming a first patterned masking layer and forming a second patterned masking layer each comprise forming a masking layer having a pattern the apertures of which are

characterized by an extent accounting for lateral dopant diffusion during the heat treatment.

11. The method of claim 1 wherein forming an electrically conducting charge transfer channel in a semiconductor substrate comprises ion implantation of a selected electrical dopant into a silicon substrate, the selected electrical dopant being of a conductivity type opposite that of the silicon substrate.

12. The method of claim 1 wherein forming an electrically insulating layer on a surface of the substrate comprises forming a layer of oxide on the substrate surface.

13. The method of claim 1 wherein forming a layer of gate electrode material on the insulating layer comprises depositing a layer of amorphous silicon on the insulating layer.

14. The method of claim 1 wherein forming a layer of gate electrode material on the insulating layer comprises depositing a layer of polysilicon on the insulating layer.

15. The method of claim 1 wherein forming a first patterned masking layer and forming a second patterned masking layer each comprise forming a layer of photoresist that is photolithographically patterned.

16. The method of claim 1 further comprising:

forming a third patterned masking layer on the gate material layer, the third patterned masking layer having apertures that expose regions of the gate material layer;

depositing a metal layer that contacts the third-pattern-exposed regions of the gate material layer; and

siliciding the gate material layer by heat treating the metal and gate material layers.

17. The method of claim 1 further comprising:

forming an electrically insulating electrode separation layer on the electrically doped and etched gate electrode material layer;

forming an upper gate electrode material layer on the insulating electrode separation layer;

forming on the upper gate material layer a third patterned masking layer having apertures that expose regions of the underlying upper gate material layer that are to form gate electrodes;

electrically doping the third-pattern-exposed regions of the upper gate material layer;

forming on the upper gate material layer a fourth patterned masking layer having apertures that expose regions of the underlying upper gate material layer that are to form gaps between gate electrodes; and

etching the fourth-pattern-exposed regions of the upper gate material layer.

18. A method of making a charge-coupled device comprising:

forming an electrically conducting charge transfer channel in a semiconductor substrate;

forming on a substrate surface a first patterned masking layer having apertures that expose regions of the underlying substrate surface that are to form gate electrodes;

electrically doping the first-pattern-exposed regions of the substrate surface;

forming on the substrate surface a second patterned masking layer having apertures that expose regions of the underlying substrate surface layer that are to form gaps between gate electrodes; and

etching the second-pattern-exposed regions of the substrate surface.

19. A method of making electrically conducting electrodes comprising:

forming an electrically insulating layer on a surface of a substrate;

forming a layer of electrode material on the insulating layer;

forming on the electrode material layer a first patterned masking layer having apertures that expose regions of the underlying electrode material layer that are to form electrodes;

electrically doping the first-patterned-exposed regions of the electrode material layer;

forming on the electrode material layer a second patterned masking layer having apertures that expose regions of the underlying electrode material layer that are to form gaps between electrodes; and

etching the second-patterned-exposed regions of the electrode material layer.

20 A method of making electrically conducting electrodes comprising:

forming on a substrate surface a first patterned masking layer having apertures that expose regions of the underlying substrate surface that are to form electrodes;

electrically doping the first-pattern-exposed regions of the substrate surface;

forming on the substrate surface a second patterned masking layer having apertures that expose regions of the underlying substrate surface layer that are to form gaps between electrodes; and

etching the second-pattern-exposed regions of the substrate surface.